UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/973,888	10/11/2001	Kazuhiro Okabayashi	60188-108	8960

			EXAMINER

7590   12/23/2004

Jack Q. Lever Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER
YANCHUS III, PAUL B

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _18 November 2004_.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under _Ex parte Quayle_, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-7_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _6_ is/are allowed.

6)☒ Claim(s) _1,2,4 and 7_ is/are rejected.

7)☒ Claim(s) _3 and 5_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _11/18/04_.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

This final office action is in response to amendments filed on 9/18/04.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi et al.,

US Patent no. 5,903,503 [Yamauchi], in view of, Bar-Niv, US Patent no. 5,631,591.

Yamauchi teaches an integrated circuit having a multiprocessor architecture, the circuit

comprising:

a first processor [EU1 in Figure 13 and column 33, line 10], which operates

synchronously with a first internal clock signal [CK1 in Figure 13];

a second processor [EU2 in Figure 13 and column 33, line 11], which operates

synchronously with a second internal clock signal [CK1 in Figure 13];

a memory [RAM in Figure 13], which operates synchronously with a third internal clock

signal [CK1 in Figure 13] ; and

a clock supply unit [SUB CLOCK GENERATOR1 in Figure 13], which generates, from

an external clock signal [CK0 in Figure 13], three clock signals that are in phase with each

other, and which supplies the clock signals as the first, second and third internal clock signals,

respectively [CK1 being supplied to EU1, EU2 and RAM in Figure 13] ;

wherein the first processor, the second processor, the memory, and the clock supply unit

are integrated together on a single chip [LSI chip, column 33, line 10 and Figure 13].

Yamauchi does not explicitly disclose adjusting the delays of the clock signals to ensure

that the clocks signals are in phase. Bar-Niv discloses adjusting the delays of a plurality of

processor clock signals to ensure that the clock signals are in phase [column 6, line 61 – column

7, line 14]. It would have been obvious to one of ordinary skill in the art to include the Bar-Niv

synchronizing circuitry into the Yamauchi integrated circuit in order to ensure that different

typed of processing chips may receive synchronized clock signals [Bar-Nov, column 3, lines 23-

30].

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi et al.,

US Patent no. 5,903,503 [Yamauchi] and Bar-Niv, US Patent no. 5,631,591, in view of

Applicant's Admitted Prior Art [AAPA].

Yamauchi and Bar-Niv teach an integrated circuit having a multiprocessor architecture

with shared memory, but do not explicitly teach the specific components of the memory and their

operations.

AAPA teaches a well known multiprocessor architecture with shared memory.

Specifically, AAPA teaches that it is well known in the art for a memory to comprise:

a memory array which is used to store data [MEMORY in Figure 10], and

a memory controller interposed between the first processor [element 500 in Figure 10]

and the memory array [MEMORY in Figure 10] and between the second processor [element

510 in Figure 10] and the memory array,

wherein the memory controller, receives a first memory access signal [MRW1 in Figure

10], a first address [ADRS1 in Figure 10], a second memory access signal [MRW2 in Figure

10] and a second address [ADRS2 in Figure 10], the first memory access signal and the first

address being output by the first processor [element 500 in Figure 10], the second memory

access signal and the second address being output by the second processor [element 510 in

Figure 10];

selects and provides the first address to the memory array when the first memory access

signal is asserted [page 3, line 19 – page 4, line 5; and

selects and provides the second address to the memory array when the second memory

access signal is asserted [page 4, lines 6-12].

It would have been obvious to one of ordinary skill in the art to include the well known

memory structure taught by AAPA into the integrated circuit taught by Yamauchi to manage

read and write requests from the plurality of processors.

Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi

et al., US Patent no. 5,903,503 [Yamauchi] and Bar-Niv, US Patent no. 5,631,591, in view of

Terashima, US Patent no. 6,289,436.

Yamauchi and Bar-Niv, as described above, teach an integrated circuit having a

multiprocessor architecture, but do not explicitly teach a reset control unit for receiving external

reset signals and generating internal reset signals for resetting system components.

Terashima teaches a reset control unit for receiving external reset request signals and selectively generating internal reset commands to the system components based on the external reset request signals and the system state [column 5, line 65 – column 6, line 62].

It would have been obvious to one of ordinary skill in the art to utilize the reset circuitry taught by Terashima with the system taught by Yamauchi in order to ensure that the proper internal components are reset in response to external reset requests.

Allowable Subject Matter

Claims 3 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 6 is allowed.

Response to Arguments

Applicant's arguments, with respect to claims 3 and 5 have been fully considered and are persuasive. The rejections of claims 3 and 5 have been withdrawn.

Applicant's arguments with respect to claims 1, 2 and 4 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Paul B Yanchus whose telephone number is (571) 272-3678. The

examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Lynne H Browne can be reached on (571) 272-3670. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
December 13, 2004

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 8800 2600